Product Description

SOC provides the H.264 decoder in three formats: IP cores for FPGAs, ASIC chipsets, and standalone all-in-one modules.

IP cores are available for both Xilinx and Altera FPGAs. SOC configures the cores according to user specifications, including I/O formats.

The SOC codec chipsets (SOC-Mcodec™) are ASIC chips based on the SOC IP cores. Standard H.264 decoder chipsets for different specifications are available.

The SOC codec modules are System-on-Module (SoM) cards, based on SOC codec IP cores, that can be connected to user devices/PCBs using a standard DDR3 memory connector.

Users have the options of using the codec IP cores, chipsets, or modules. If IP cores are preferred, users have the option of Xilinx or Altera FPGAs.

SOC also offers product development boards, which allow users to develop products using the SOC codec IP core, chipsets, and modules.

Specifications

- **Standard:** H.264/AVC (ISO/IEC14496-10)
- **Profiles:** High, up to level 4.1
- Support lower profiles
- **Video resolutions:** Up to 1080i/p
- **Frame rate:** Up to 60fps
- **Chroma formats:** 4:2:2 or 4:2:0
- **Precision:** 8 bits or 10 bits
- **Input format:** H.264 Elementary, or Transport Stream
- **Video output format:** RGB or YUV
- **Audio support:** AAC or MPEG-2 Layer-II
- **Latency:** 0.25ms
- **Power consumption:** 800mw (IP core)
- **FPGAs:** Xilinx or Altera

FPGA Resources

<table>
<thead>
<tr>
<th>Logic Resources</th>
<th>Xilinx FPGAs</th>
<th>Altera FPGAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rankin Street, Waterloo, Ontario, Canada N2V 1V9</td>
<td>45,000 LUTs</td>
<td>30,000 ALMs</td>
</tr>
<tr>
<td>Block RAMs:</td>
<td>3,000kb</td>
<td>2,500kbits</td>
</tr>
<tr>
<td>DSPs:</td>
<td>25 DSPs</td>
<td>25 DSPs</td>
</tr>
</tbody>
</table>

H.264 Video/Audio Decoder Chipset

H.264 Video/Audio Decoder Module

H.264 Compressed Stream

Support multiple channels

Digital Video/Audio Data